

Fig. 1

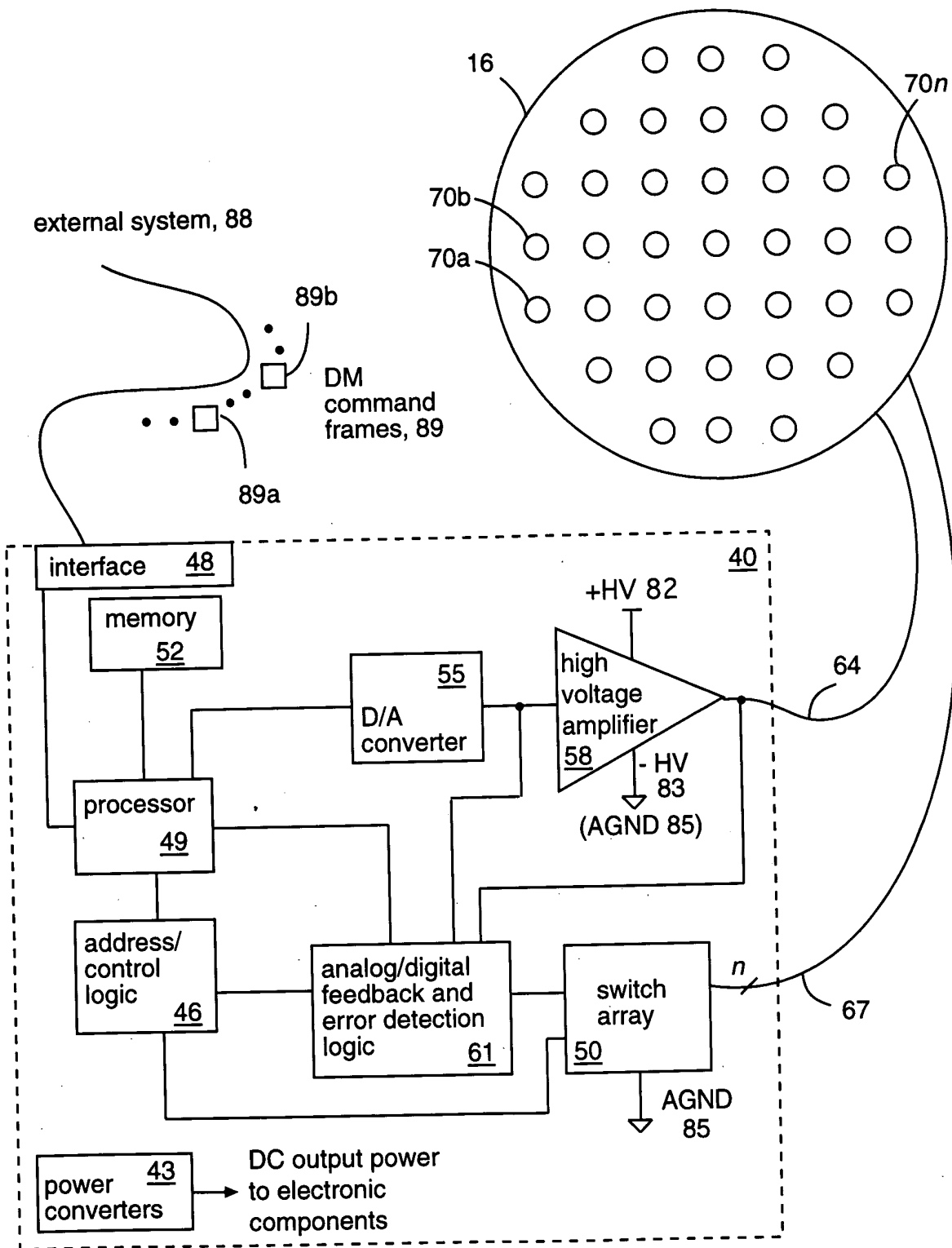


Fig. 2

The diagram illustrates a four-channel system (41a, 41b, 41c, 41d) connected to a central circular array (16). Each channel includes a D/A converter, processor, address/control logic, and switch array, all connected to a common ground (85). The central array has four zones (A, B, C, D) and is connected to an external system (88) via a master processor (45).

Channel 41a: Includes a D/A converter A, processor A, address/control logic A, and switch array A. A high voltage amplifier A is connected to the switch array A. The switch array A is connected to the central array (16) via a line labeled 64. The high voltage amplifier A is connected to the central array (16) via a line labeled 58. The D/A converter A is connected to the processor A via a line labeled 55. The processor A is connected to the address/control logic A via a line labeled 49. The address/control logic A is connected to the switch array A via a line labeled 46. The switch array A is connected to ground (85) via a line labeled 67.

Channel 41b: Includes a D/A converter B, processor B, address/control logic B, and switch array B. A high voltage amplifier B is connected to the switch array B. The switch array B is connected to the central array (16) via a line labeled 64. The high voltage amplifier B is connected to the central array (16) via a line labeled 58. The D/A converter B is connected to the processor B via a line labeled 55. The processor B is connected to the address/control logic B via a line labeled 49. The address/control logic B is connected to the switch array B via a line labeled 46. The switch array B is connected to ground (85) via a line labeled 67.

Channel 41c: Includes a D/A converter C, processor C, address/control logic C, and switch array C. A high voltage amplifier C is connected to the switch array C. The switch array C is connected to the central array (16) via a line labeled 64. The high voltage amplifier C is connected to the central array (16) via a line labeled 58. The D/A converter C is connected to the processor C via a line labeled 55. The processor C is connected to the address/control logic C via a line labeled 49. The address/control logic C is connected to the switch array C via a line labeled 46. The switch array C is connected to ground (85) via a line labeled 67.

Channel 41d: Includes a D/A converter D, processor D, address/control logic D, and switch array D. A high voltage amplifier D is connected to the switch array D. The switch array D is connected to the central array (16) via a line labeled 64. The high voltage amplifier D is connected to the central array (16) via a line labeled 58. The D/A converter D is connected to the processor D via a line labeled 55. The processor D is connected to the address/control logic D via a line labeled 49. The address/control logic D is connected to the switch array D via a line labeled 46. The switch array D is connected to ground (85) via a line labeled 67.

Central Array (16): A circular array with four zones (A, B, C, D) and a central column of points. The zones are labeled ZONE A, ZONE B, ZONE C, and ZONE D. The central column of points is labeled 70n. The array is connected to an external system (88) via a master processor (45). The array is also connected to the four channels (41a, 41b, 41c, 41d) via lines labeled 64 and 58. The array is connected to ground (85) via a line labeled 70a. The array is connected to the external system (88) via a line labeled 70b.

Master Processor (45): A master processor connected to the external system (88) and the central array (16). The master processor is connected to the external system (88) via a line labeled 88. The master processor is connected to the central array (16) via a line labeled 70b.

Fig. 3

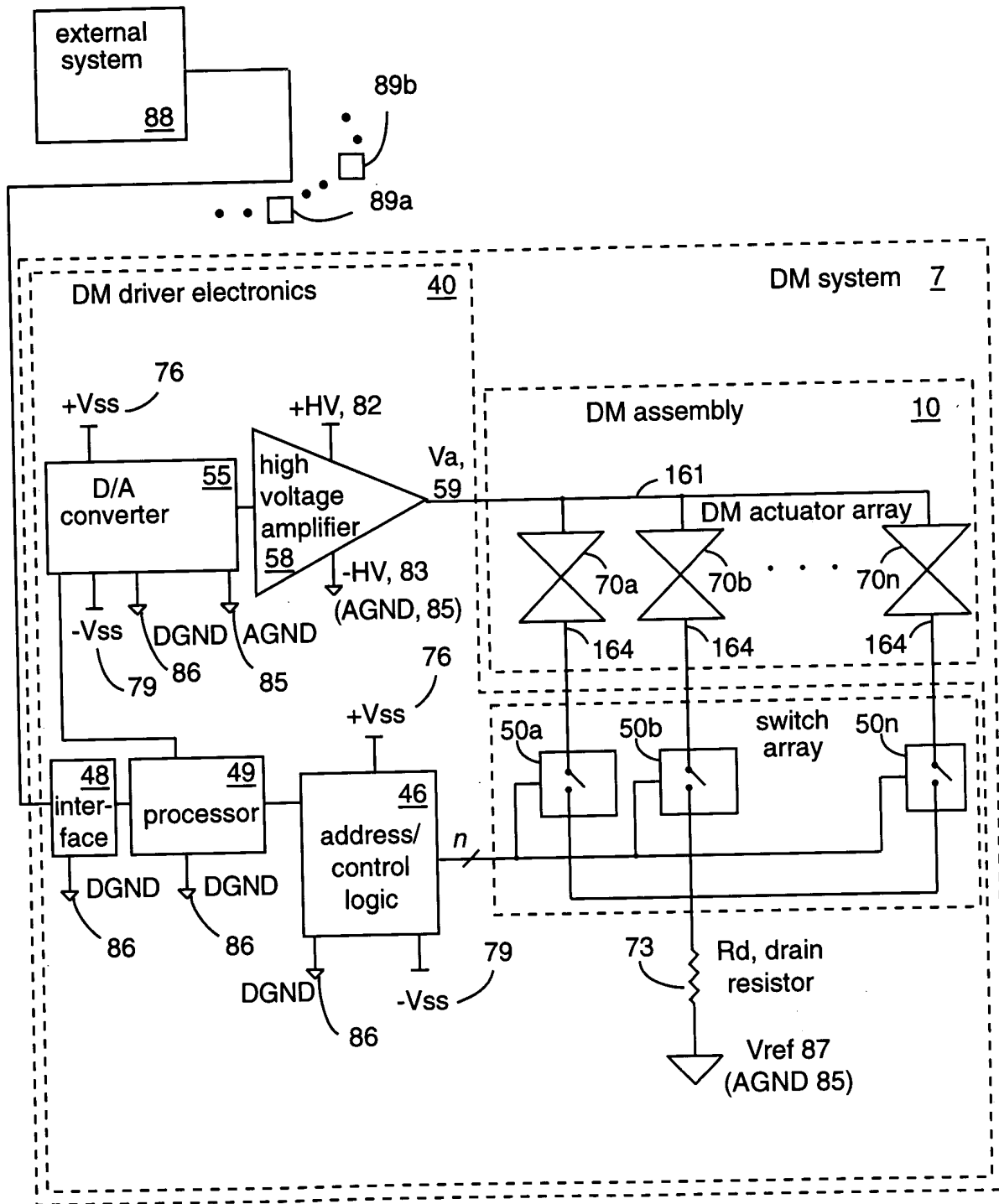


Fig. 4

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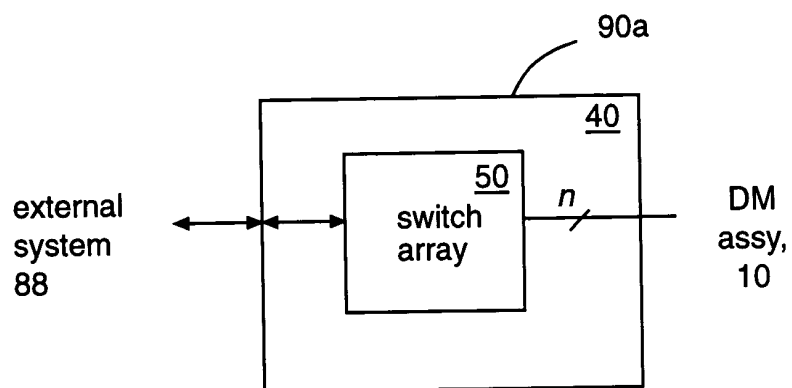


Fig. 5A

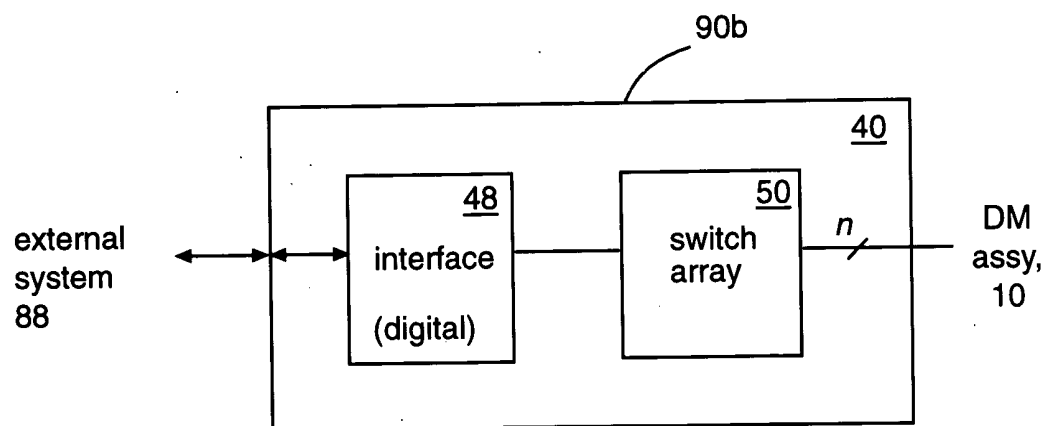


Fig. 5B

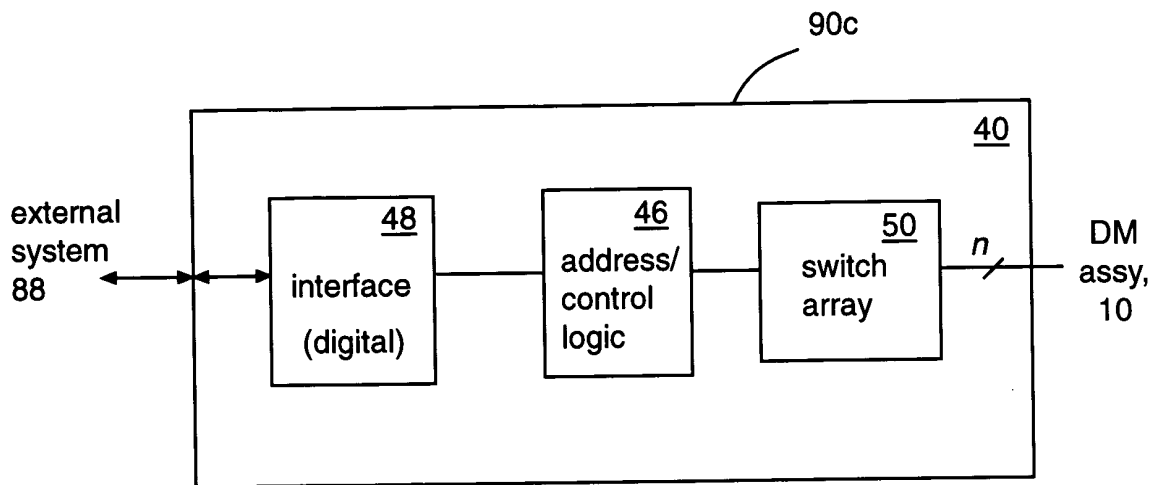


Fig. 5C

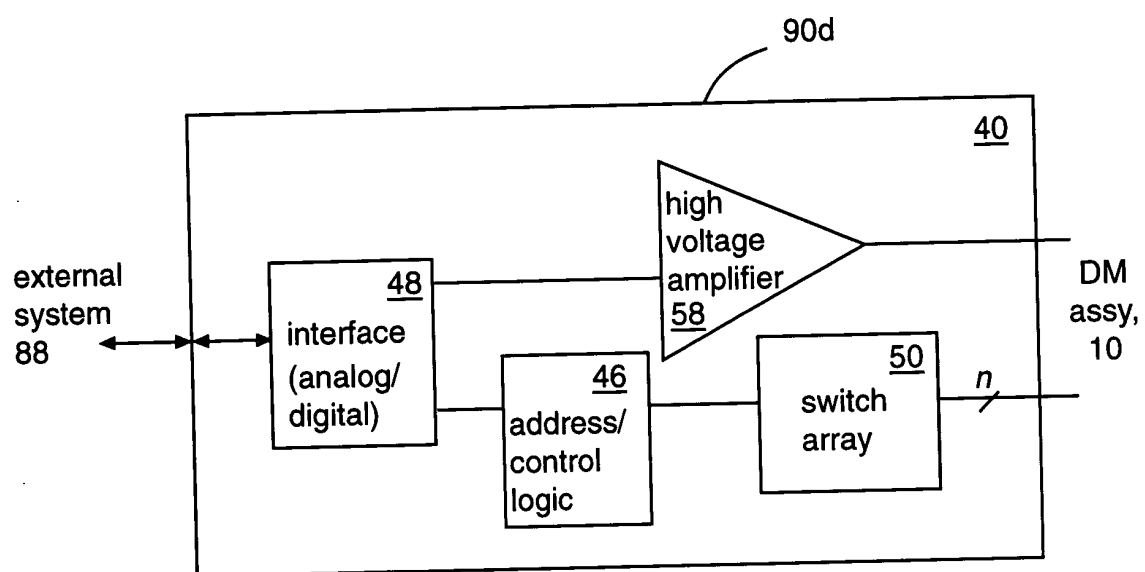
[illegible]

Fig. 5D

The diagram shows a system 90e enclosed in a rectangular box 40. On the left, an 'external system 88' is connected to an 'interface (digital) 48' via a bidirectional arrow. The interface 48 is connected to two blocks: a 'D/A converter 55' and 'address/control logic 46'. The D/A converter 55 is connected to a 'high voltage amplifier 58', which is represented by a triangle. The address/control logic 46 is connected to a 'switch array 50'. The high voltage amplifier 58 outputs to a line labeled 'DM assy, 10'. The switch array 50 outputs to a line labeled 'n' with a diagonal slash.

Fig. 5E

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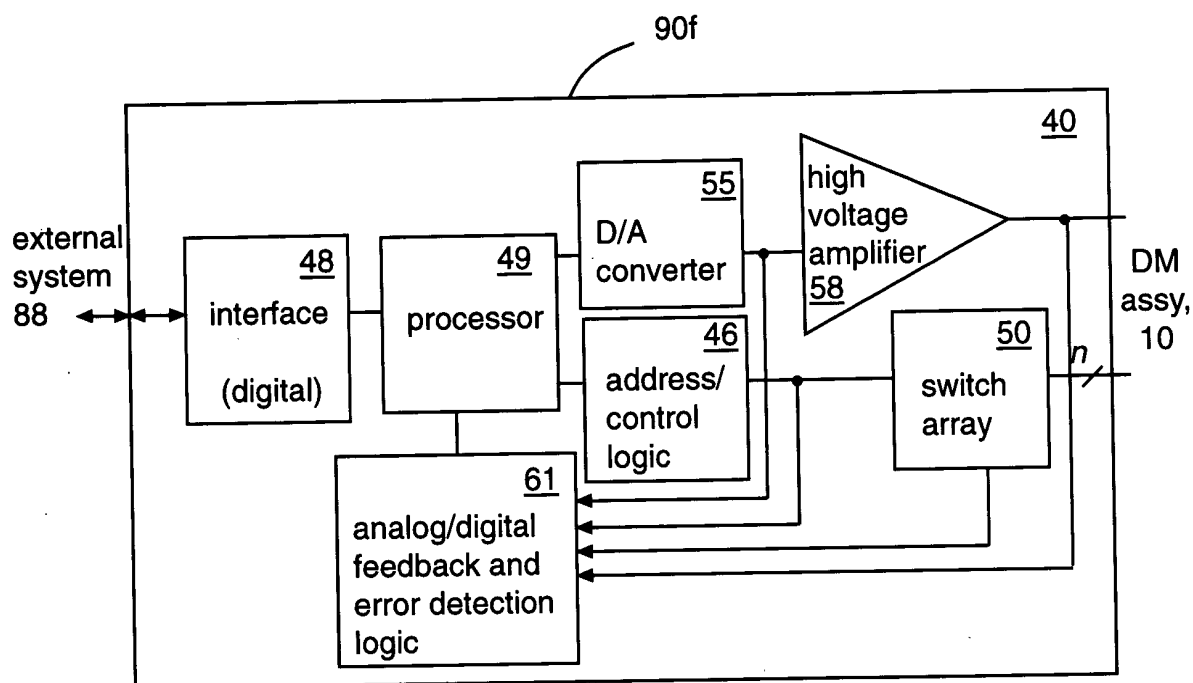


Fig. 5F

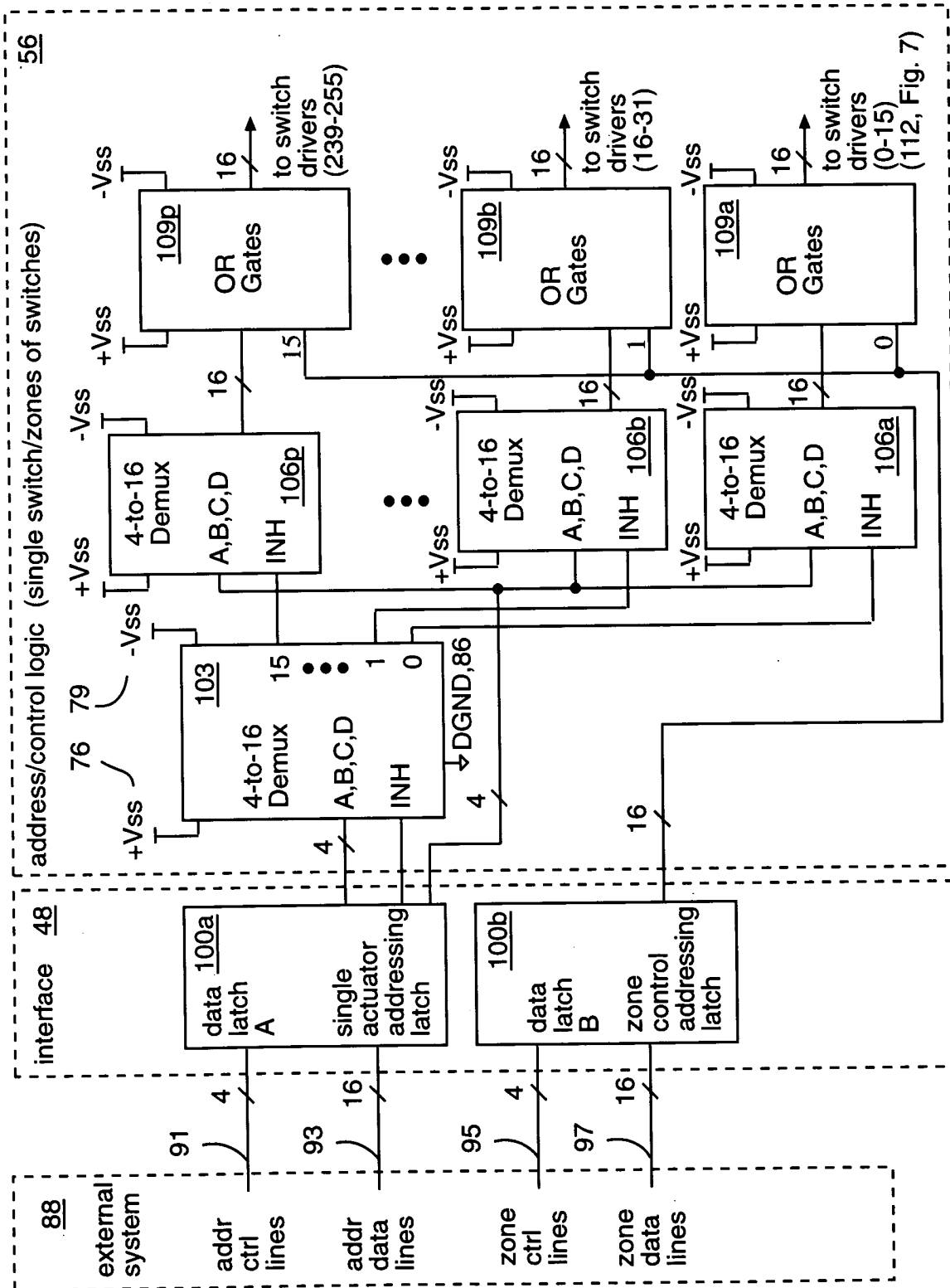


Fig. 6

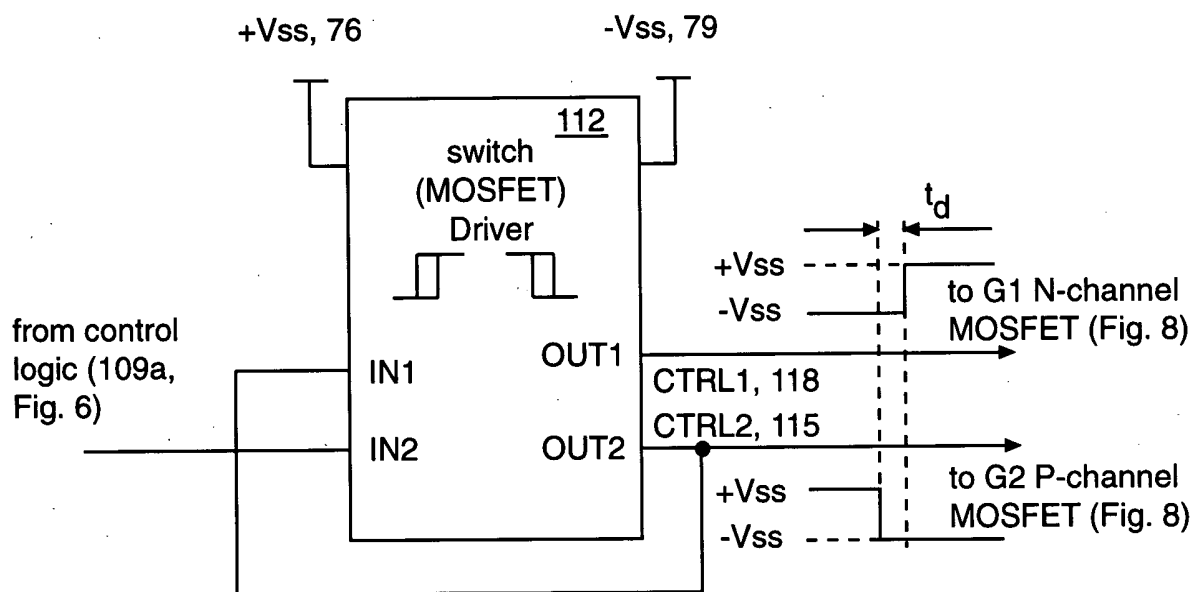


Fig. 7



Fig. 8

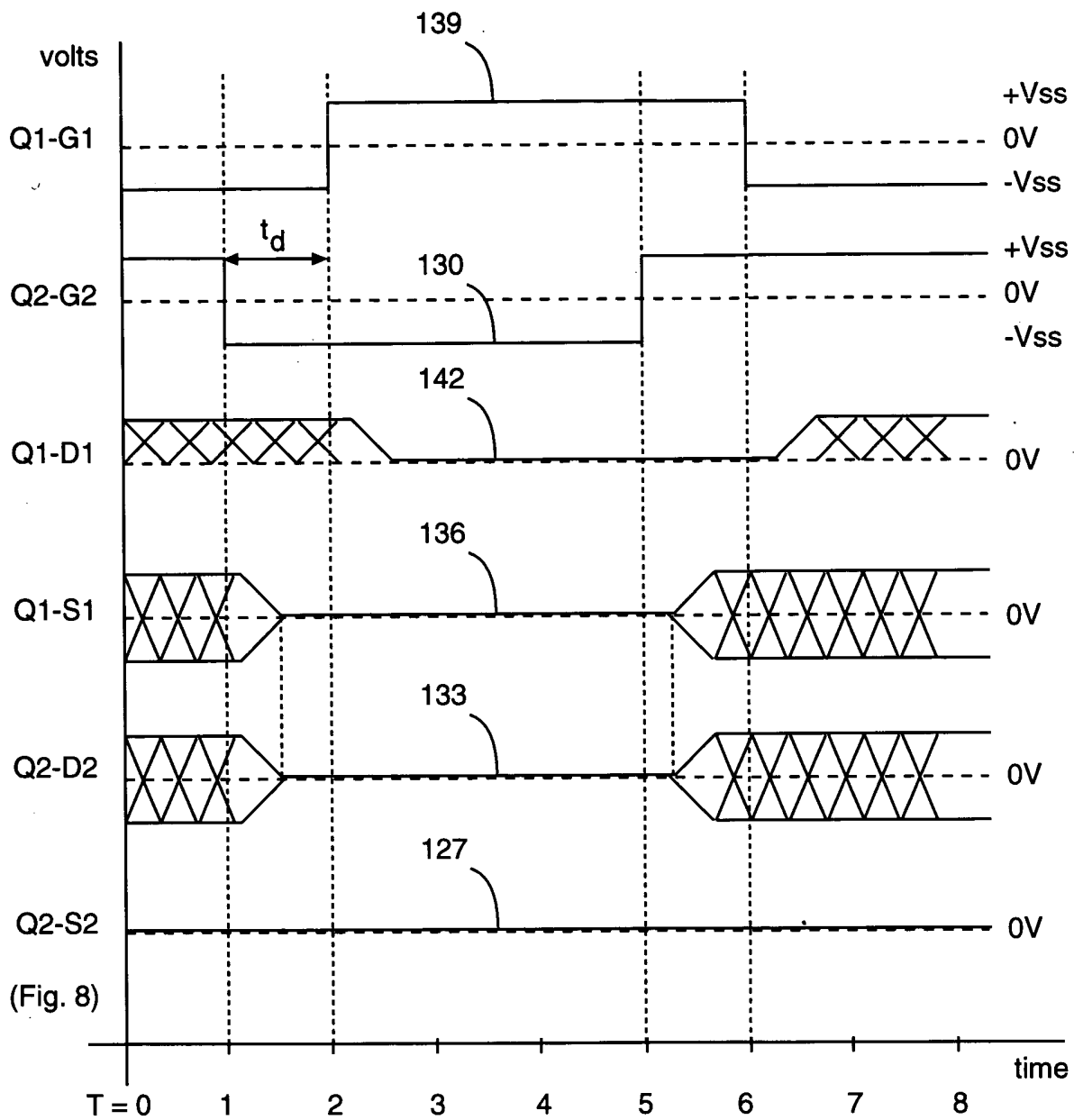


Fig. 9

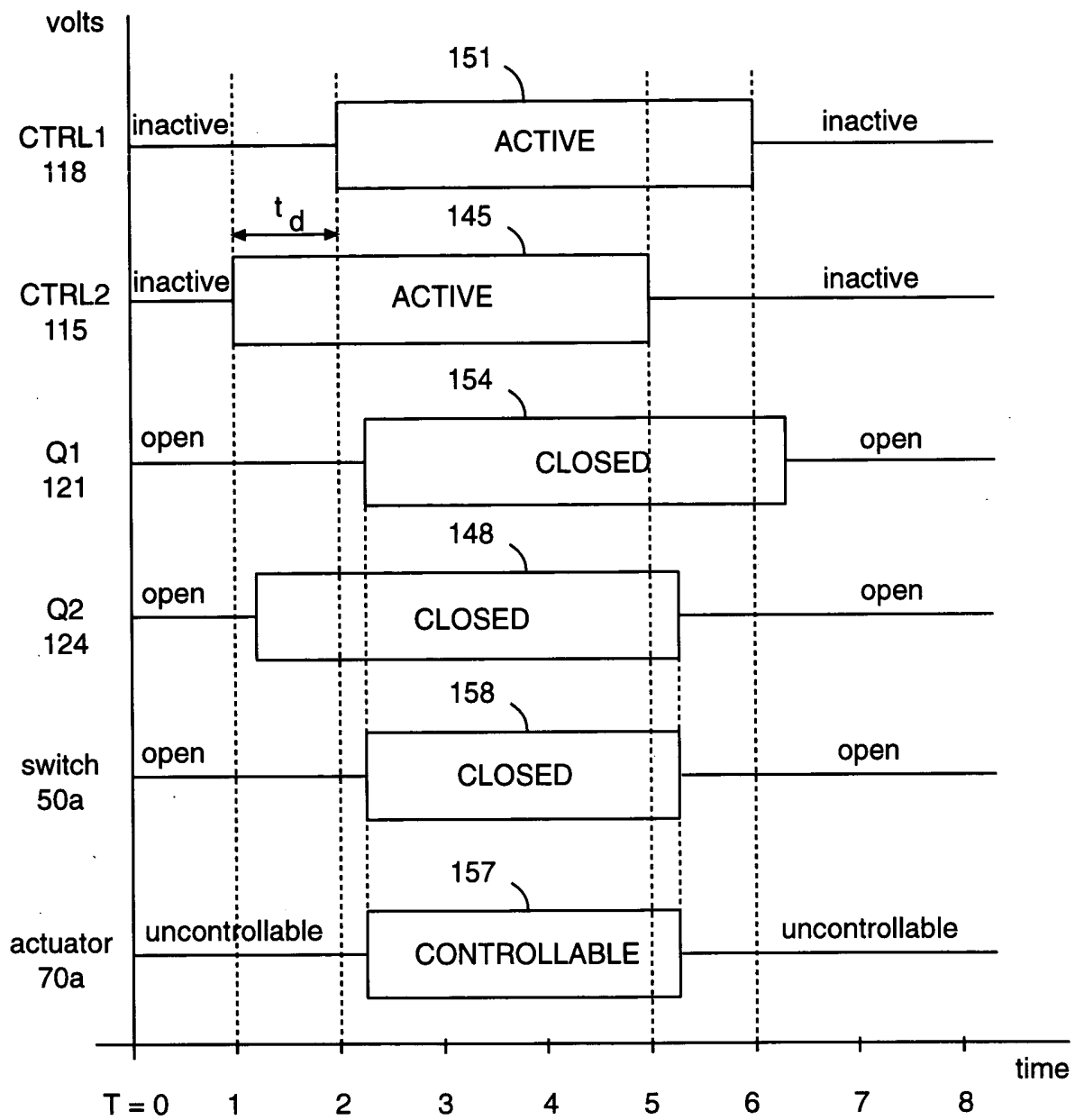


Fig. 10

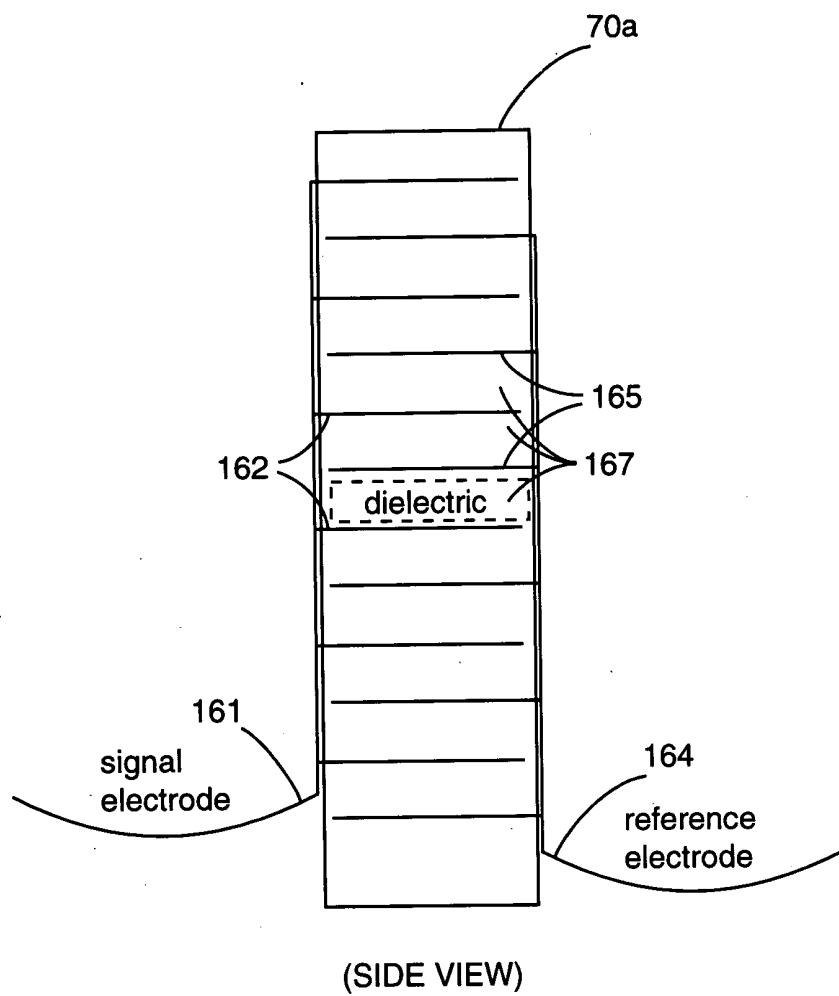


Fig. 11A

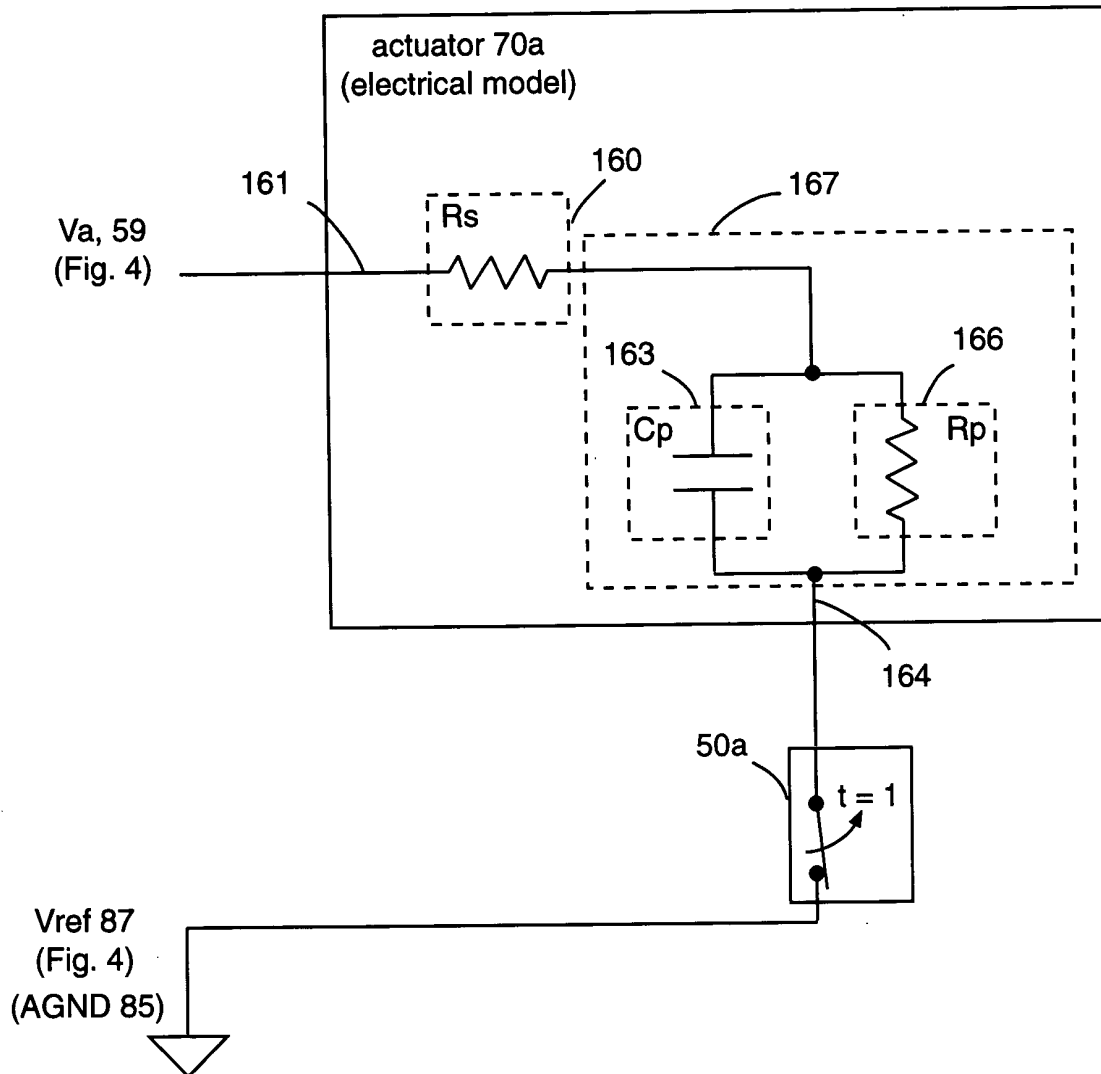


Fig. 11B

Figure 1 is a block diagram of a high voltage actuator system. The system includes a high voltage amplifier 58, a switch protection circuitry 178, and an actuator 70a. The amplifier 58 has inputs +HV 82, +40V, 0V ± 10V, and -HV 83, and an output Va, 59 (0V ± 30V). The switch protection circuitry 178 contains a switch 181 with terminals D, S, and G, and a control input ctrl with levels ±15V, ±5V, and ±3.3V. The actuator 70a is connected to the switch output and has a -70V reference Vref, 87. A detailed view 175 shows the internal structure of the switch protection circuitry, featuring an N-channel MOSFET Q with drain D, source S, and gate G, and a diode connected between D and S. Voltage levels 200V and 20V are indicated for the MOSFET and diode respectively.

Fig. 13

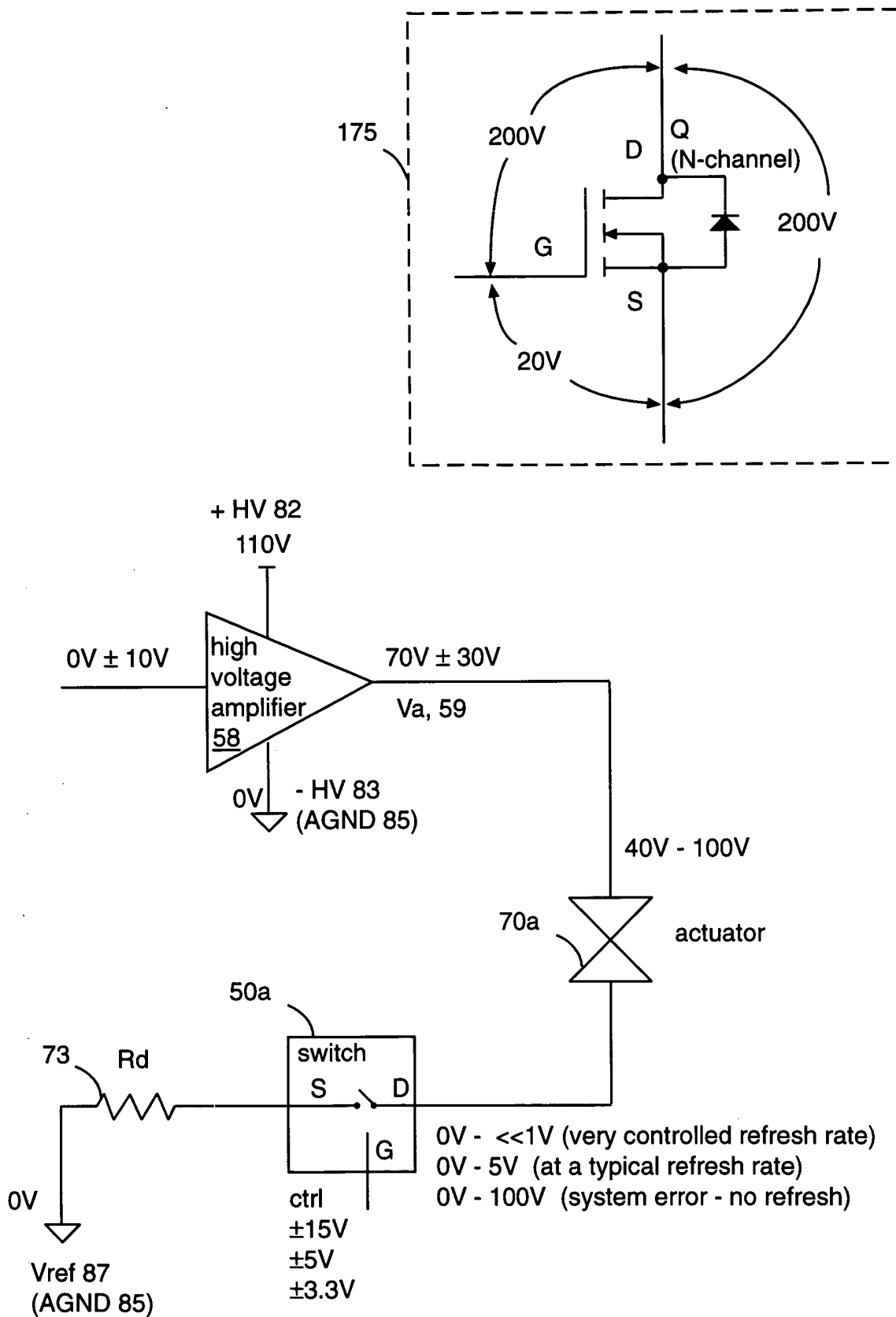


Fig. 14

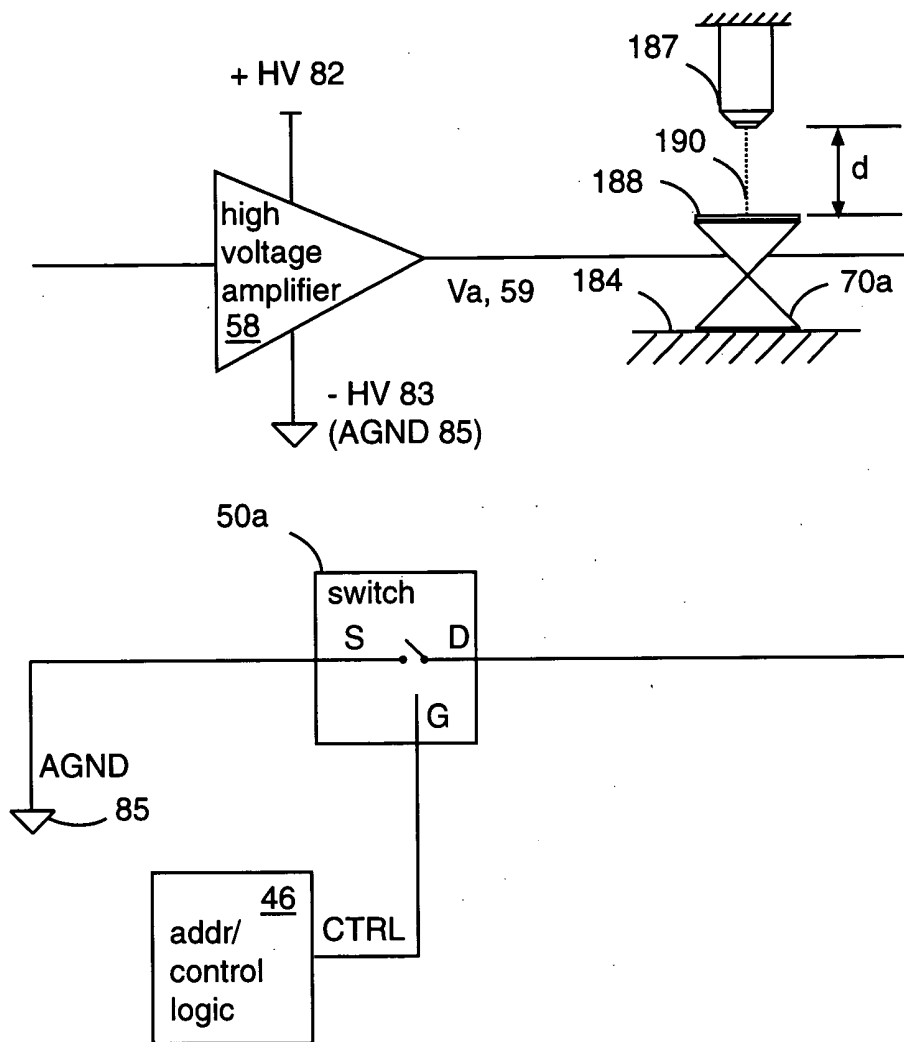


Fig. 15

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(SIDE VIEW)

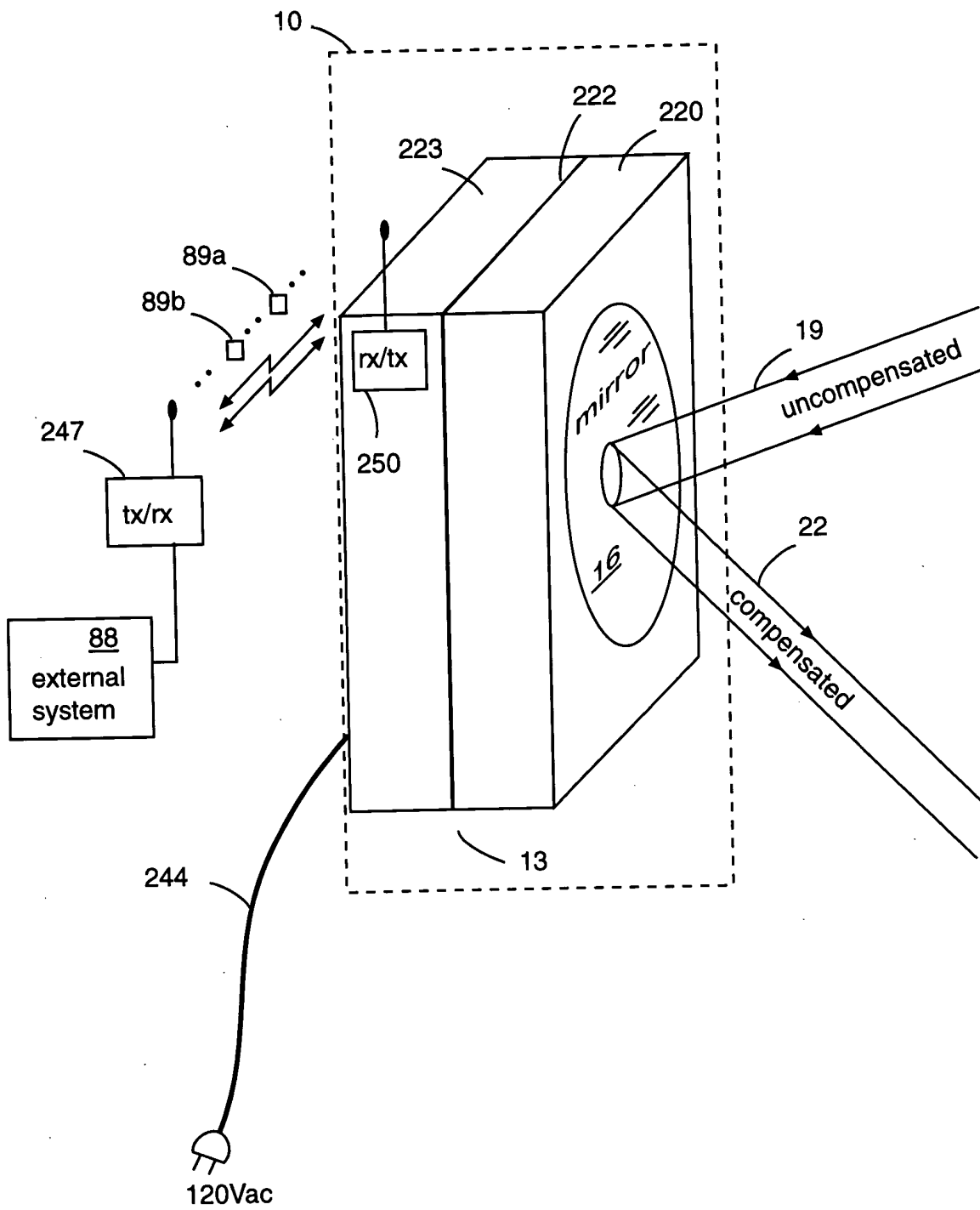


Fig. 19

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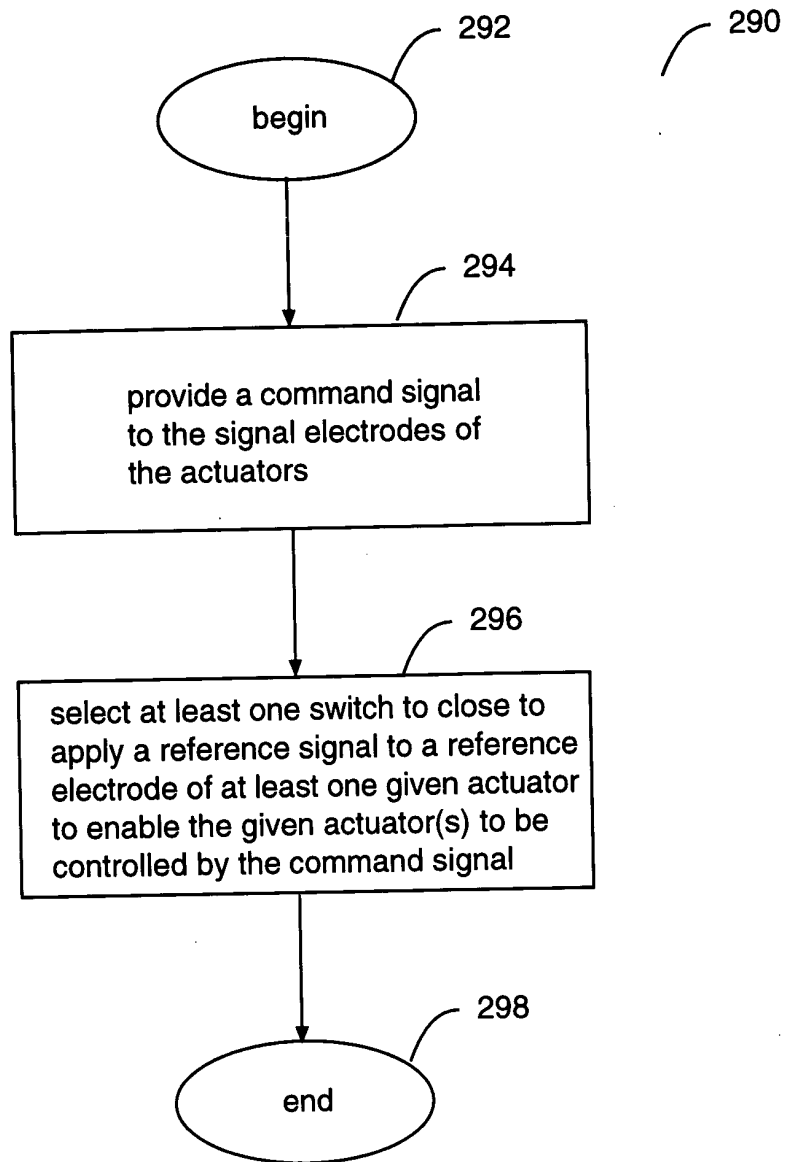


Fig. 20A

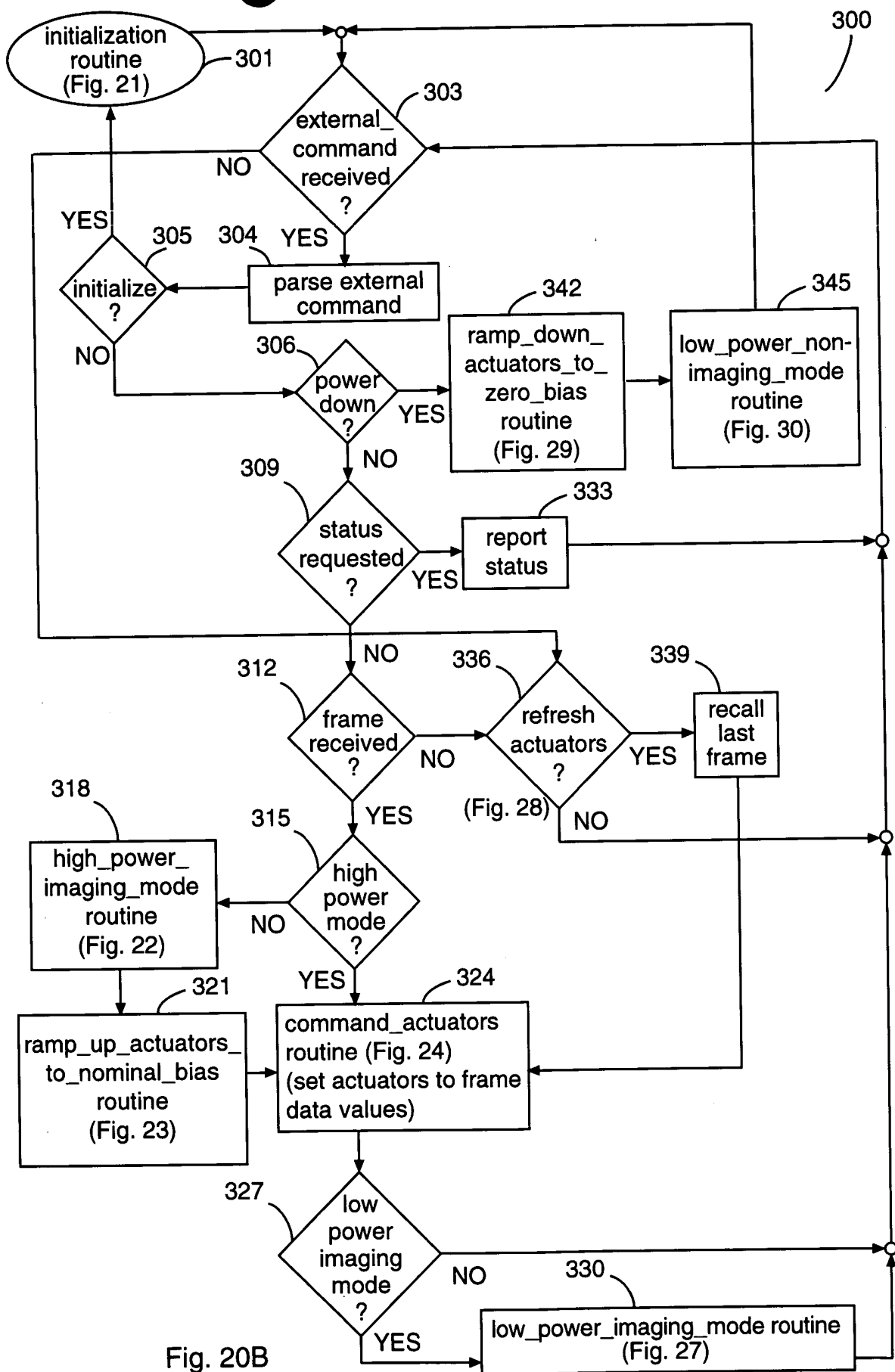


Fig. 20B

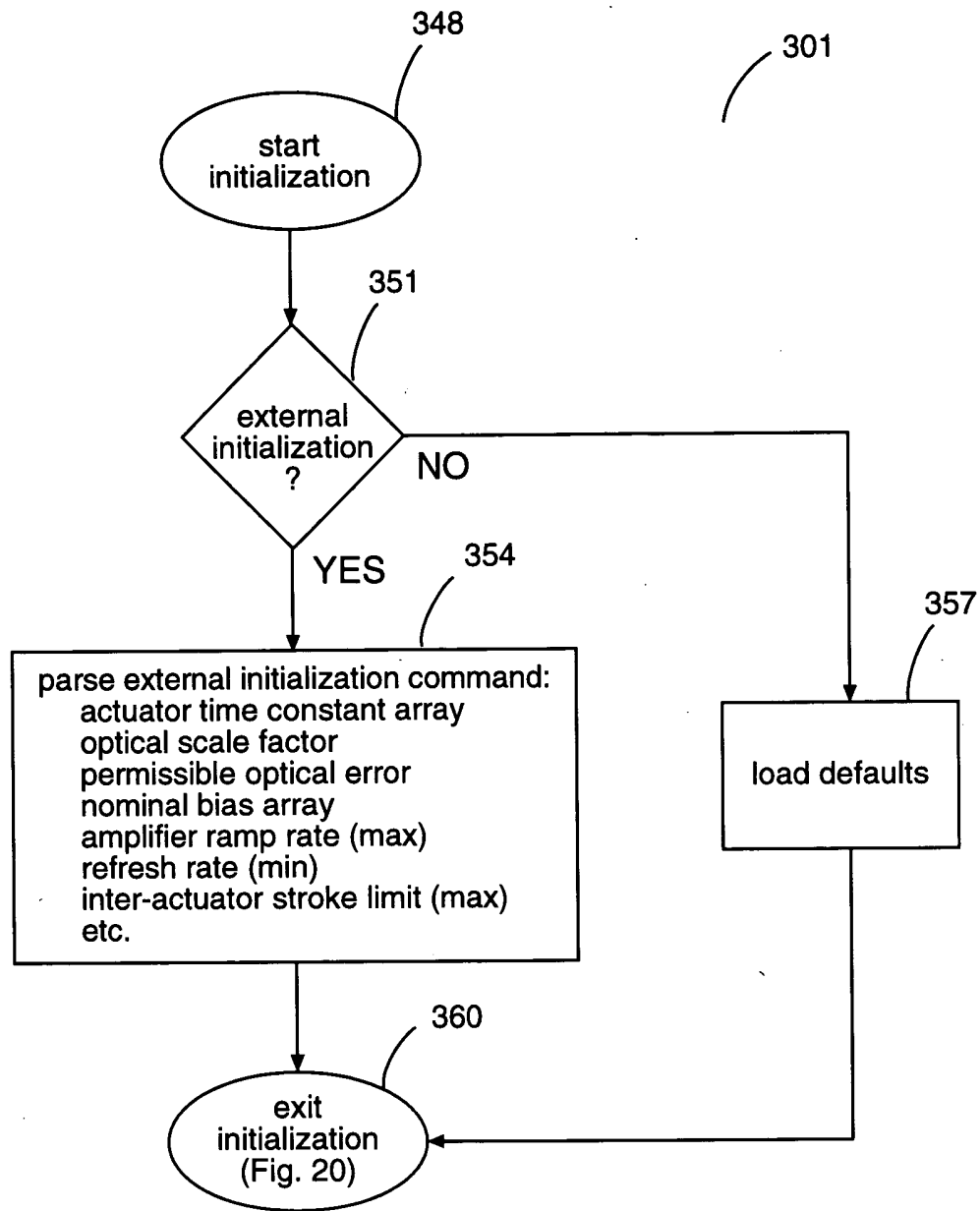


Fig. 21

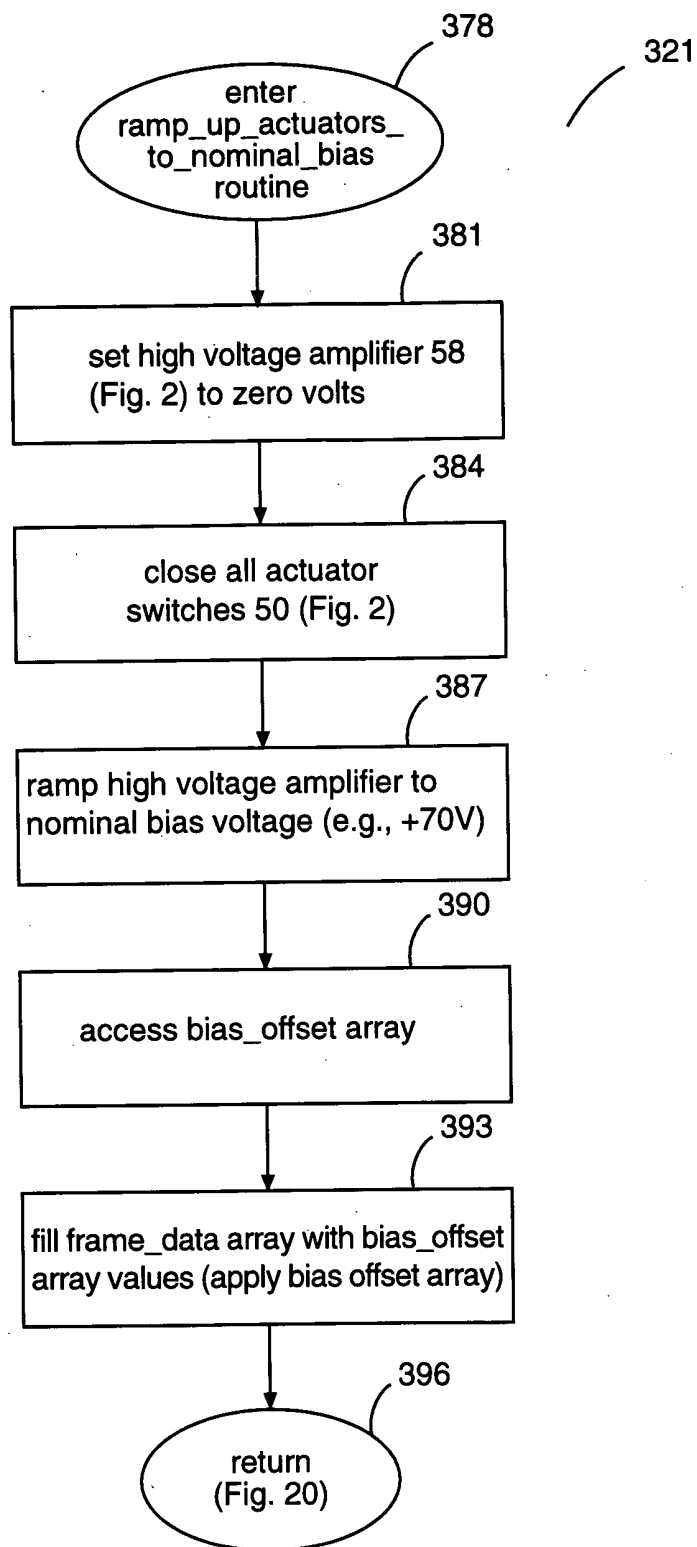


Fig. 23

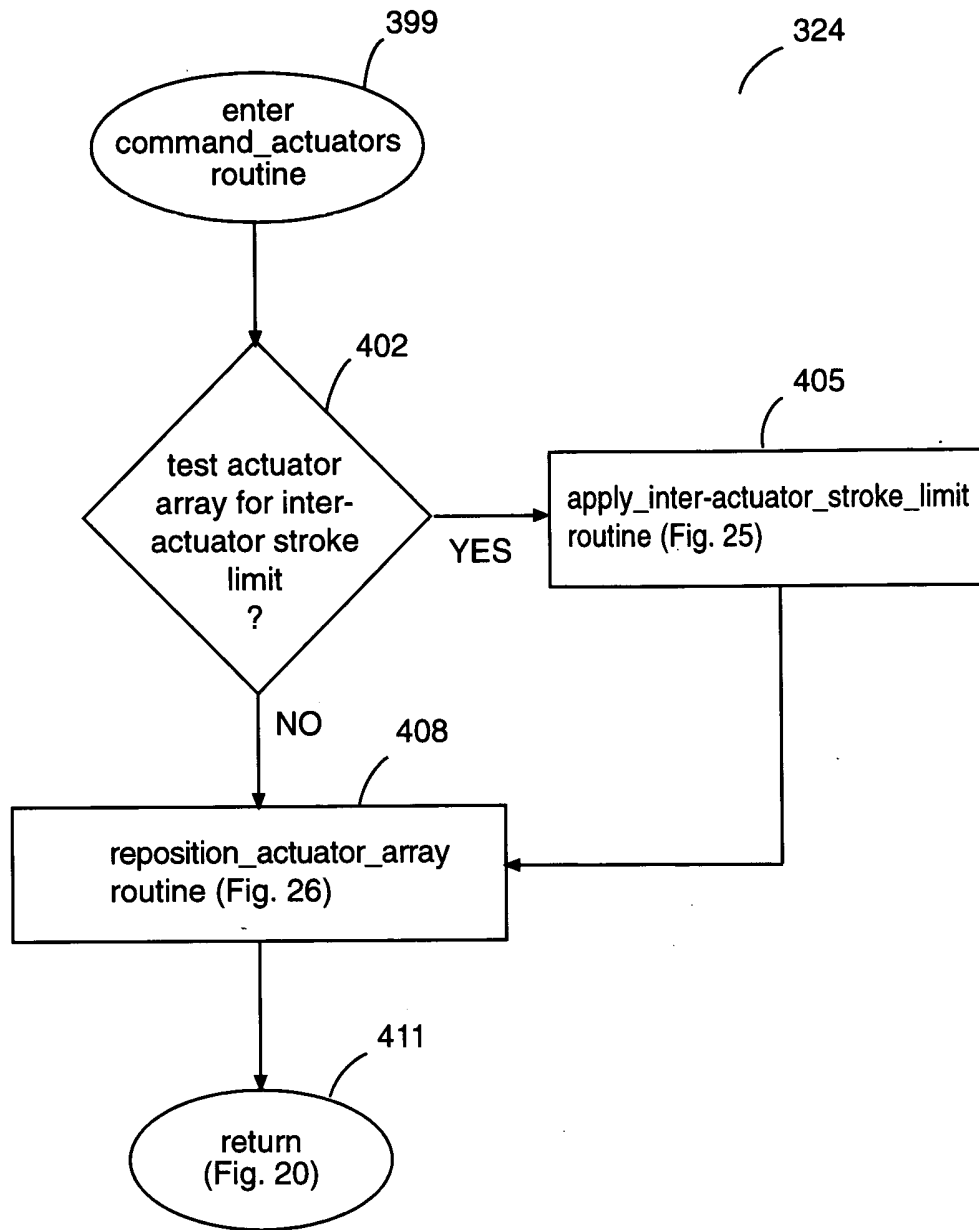


Fig. 24

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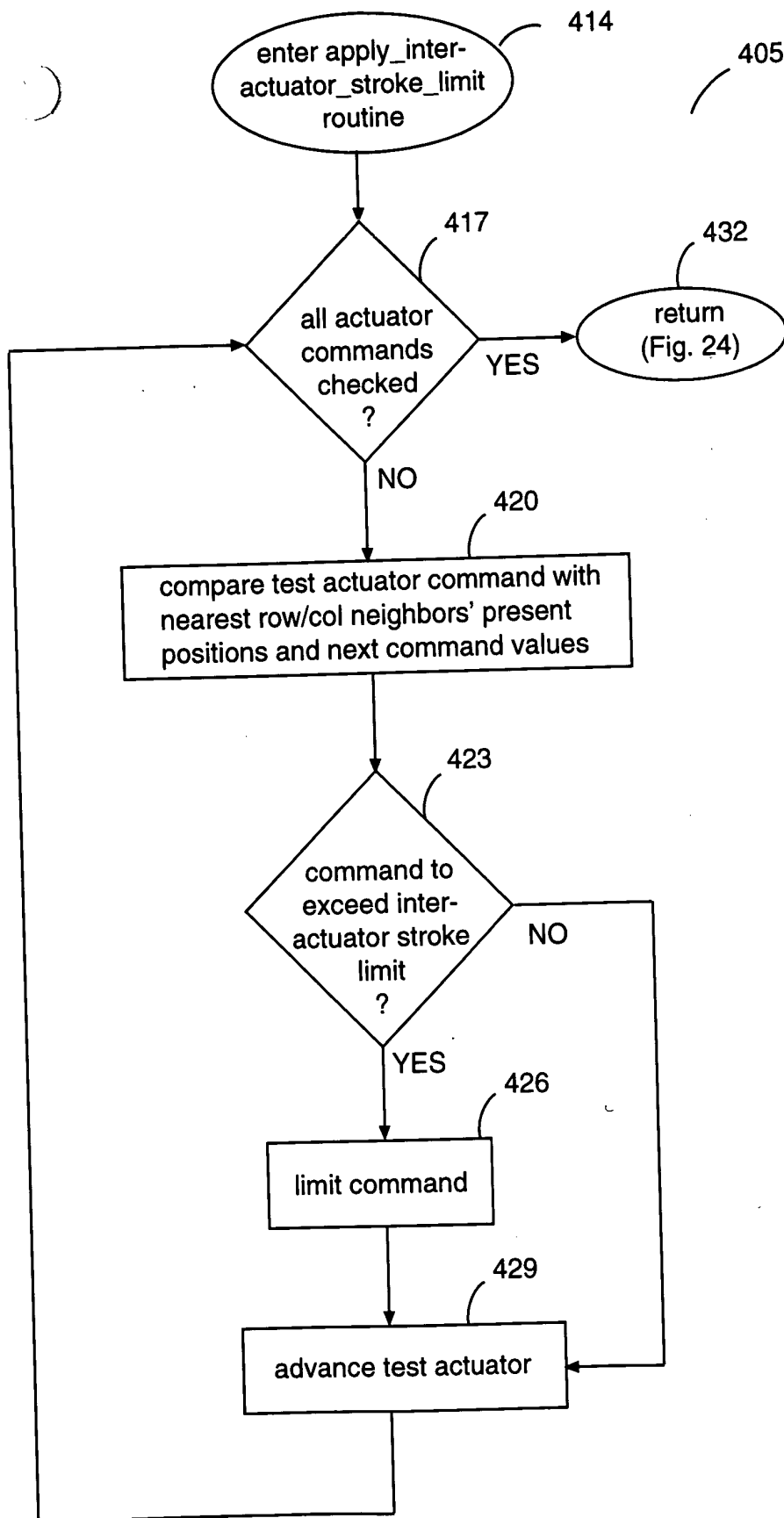


Fig. 25

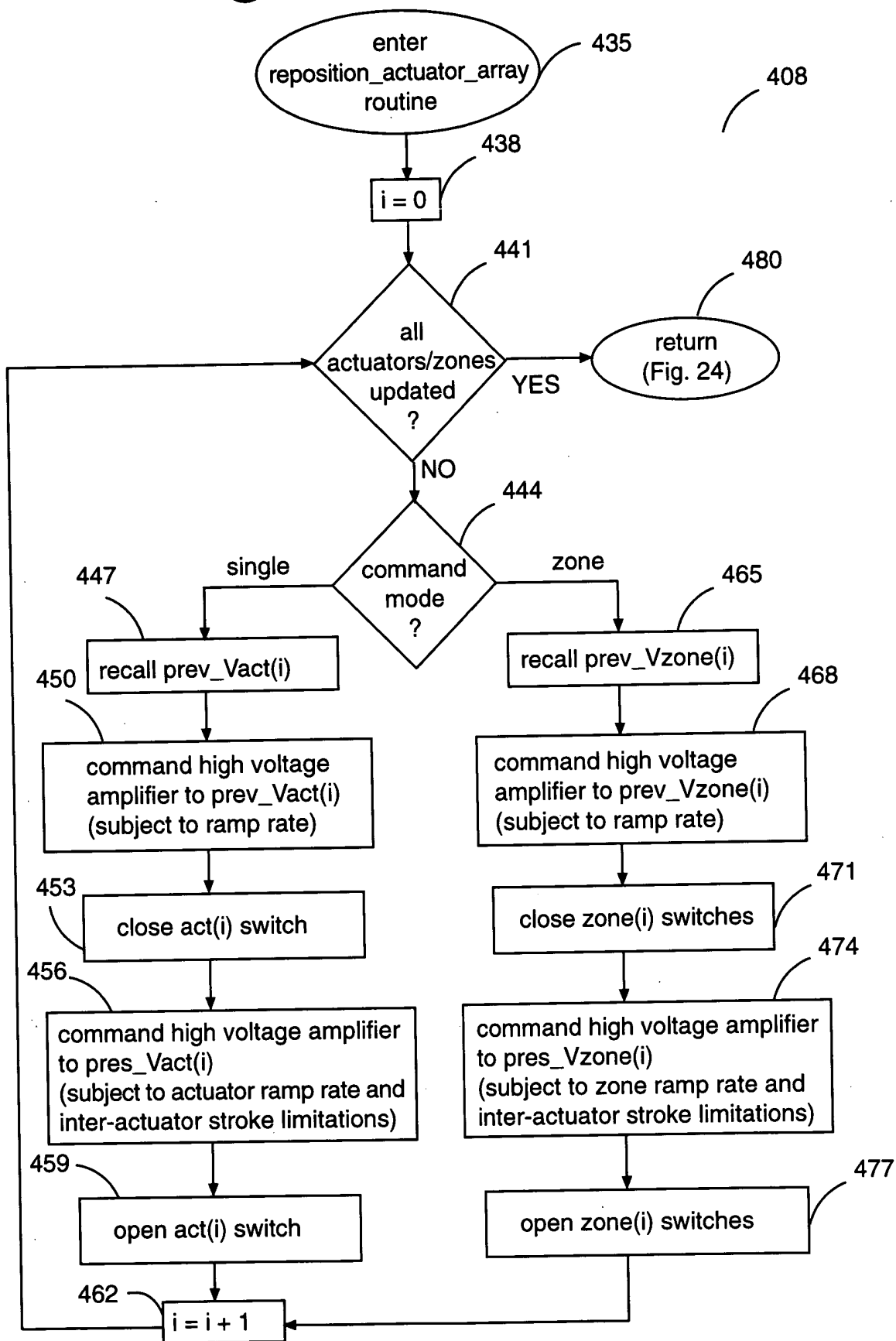


Fig. 26

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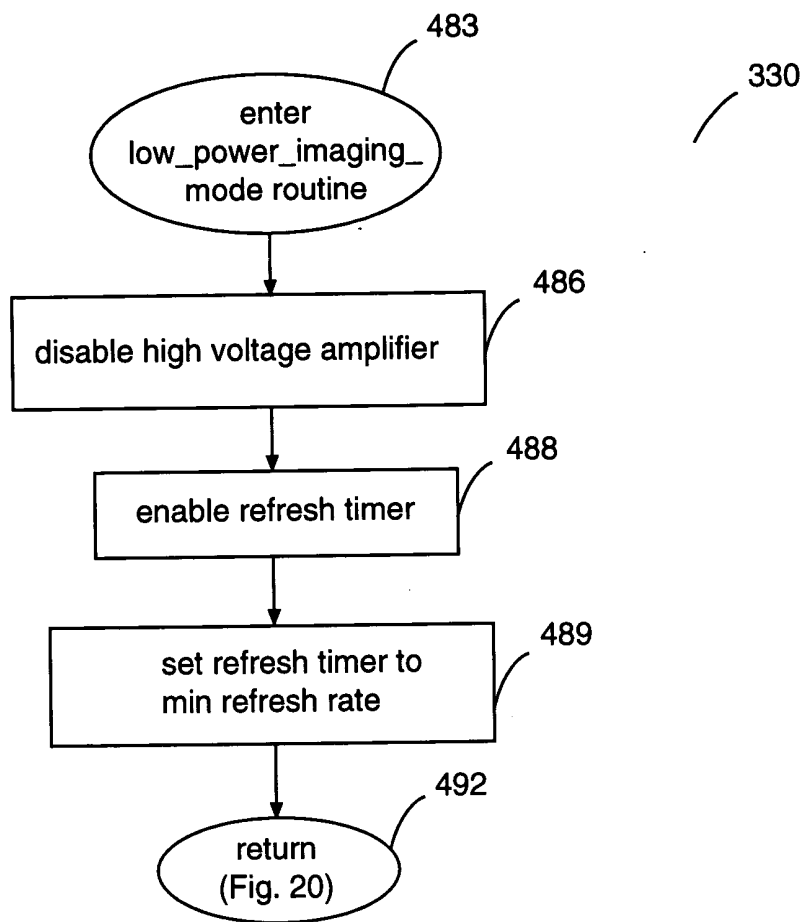


Fig. 27

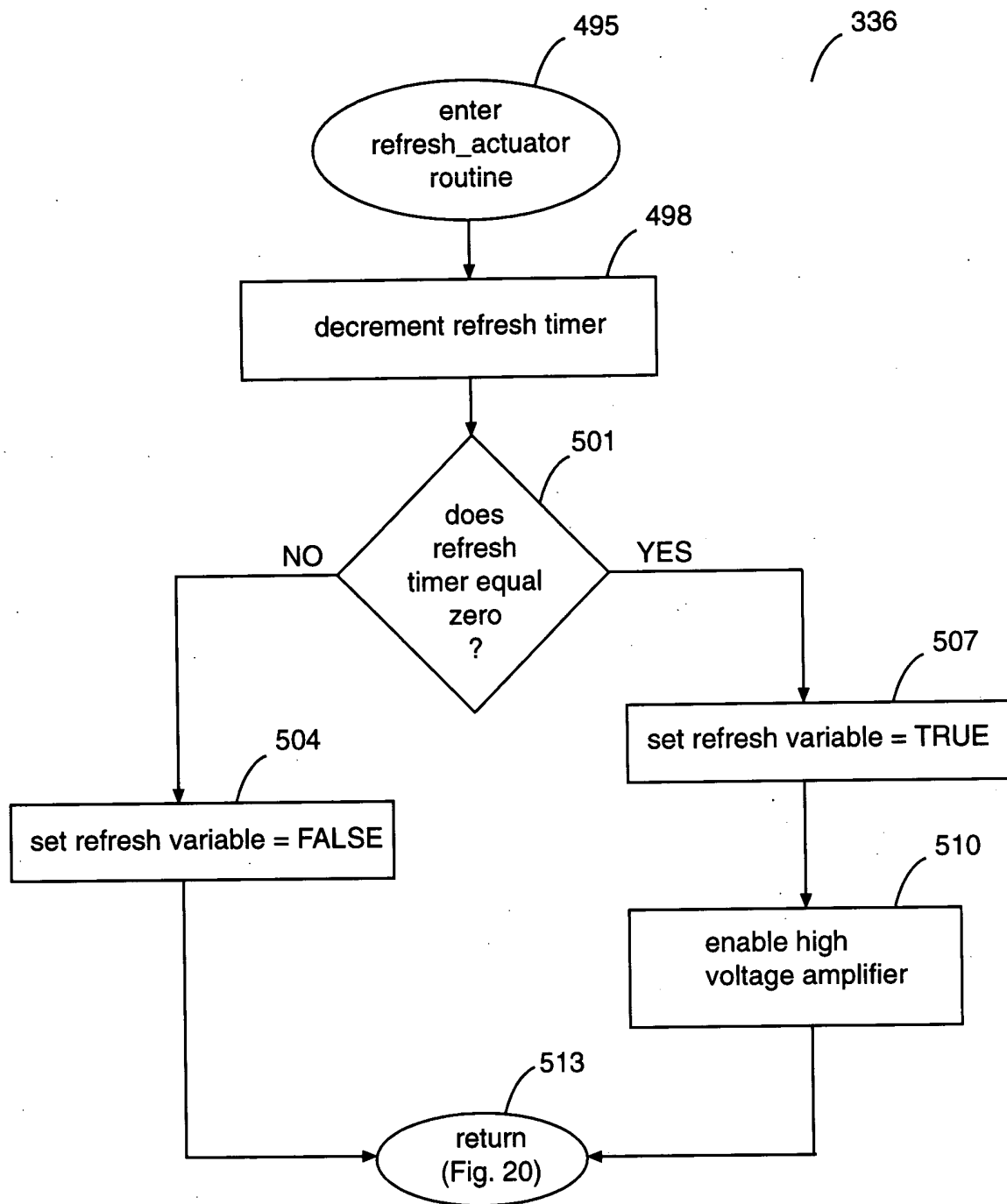


Fig. 28

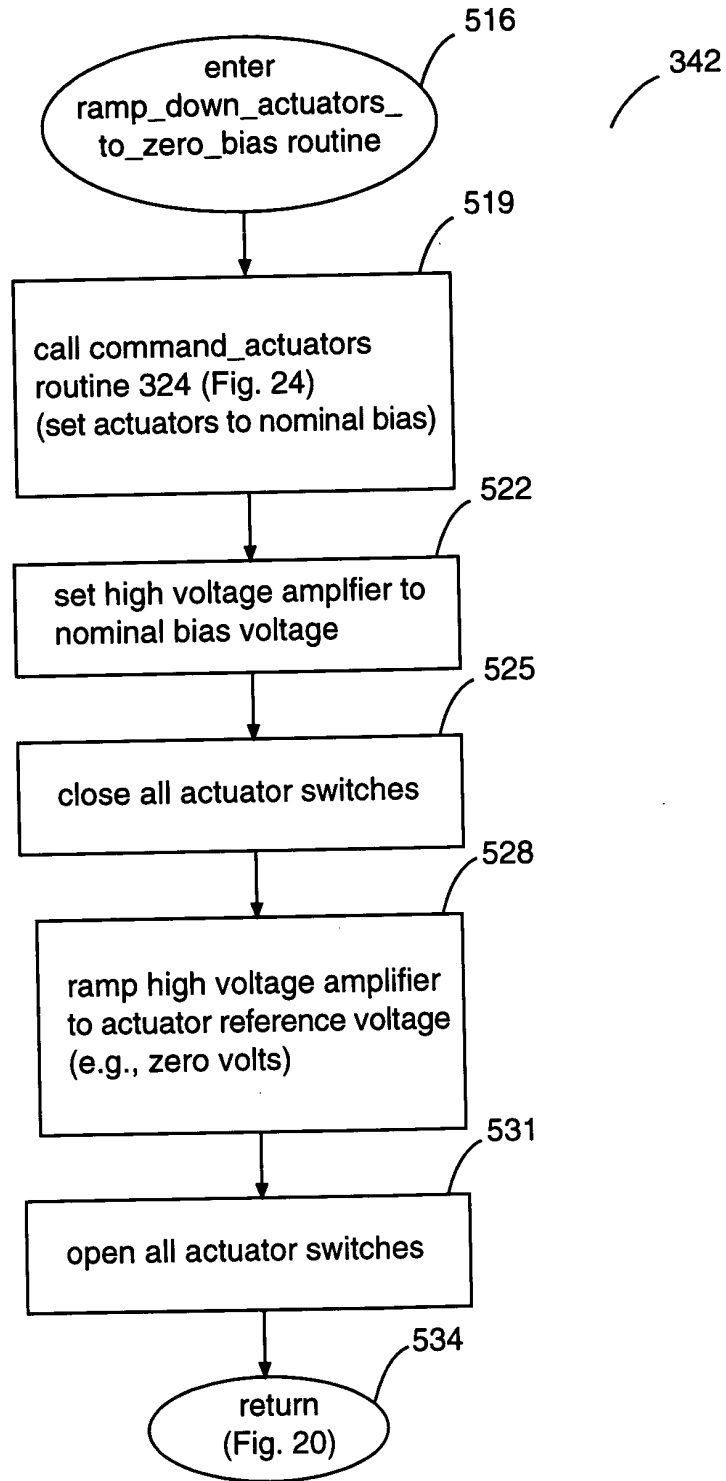


Fig. 29

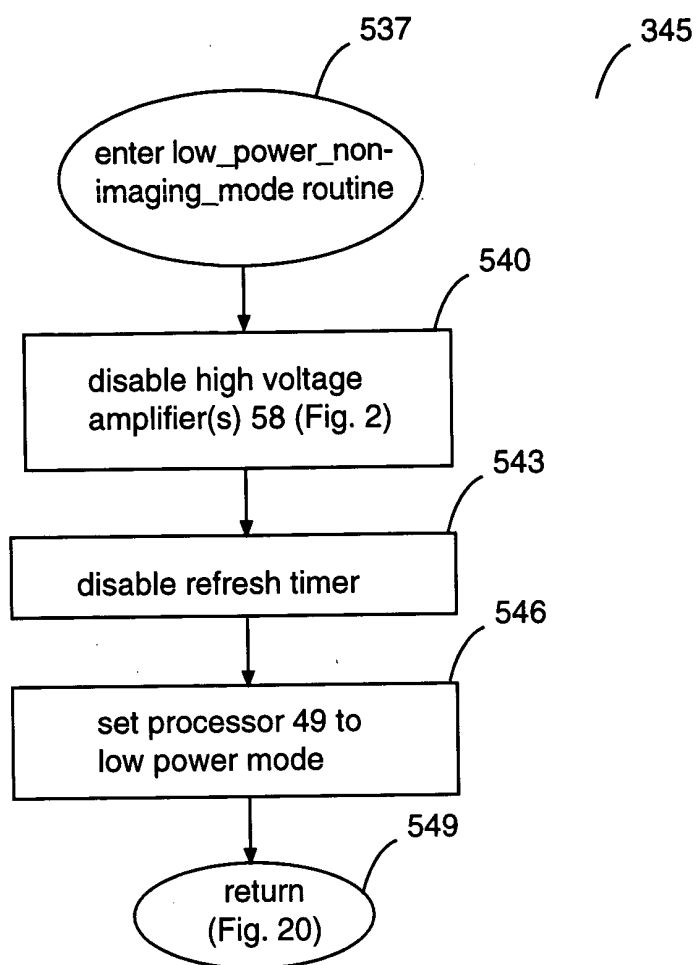


Fig. 30

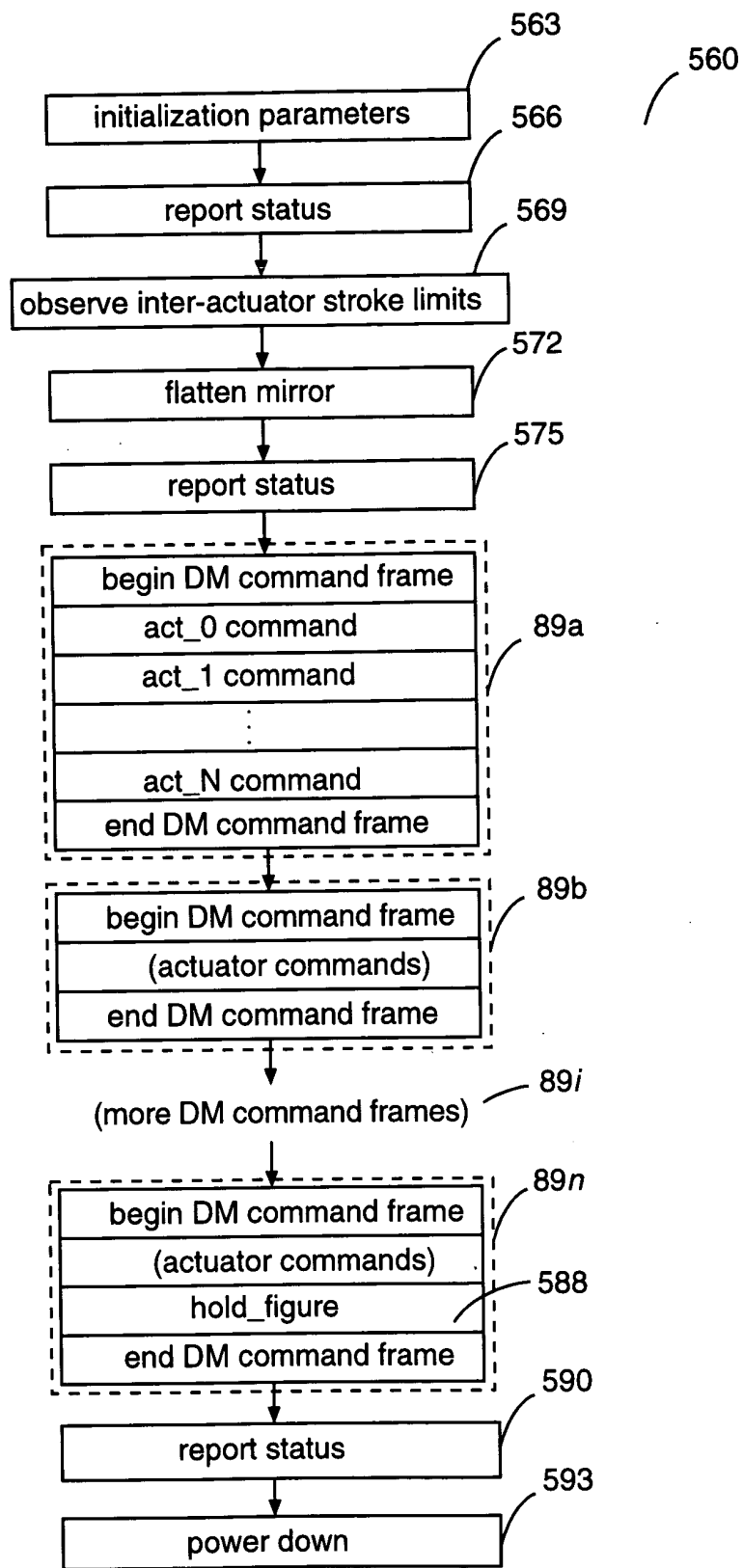
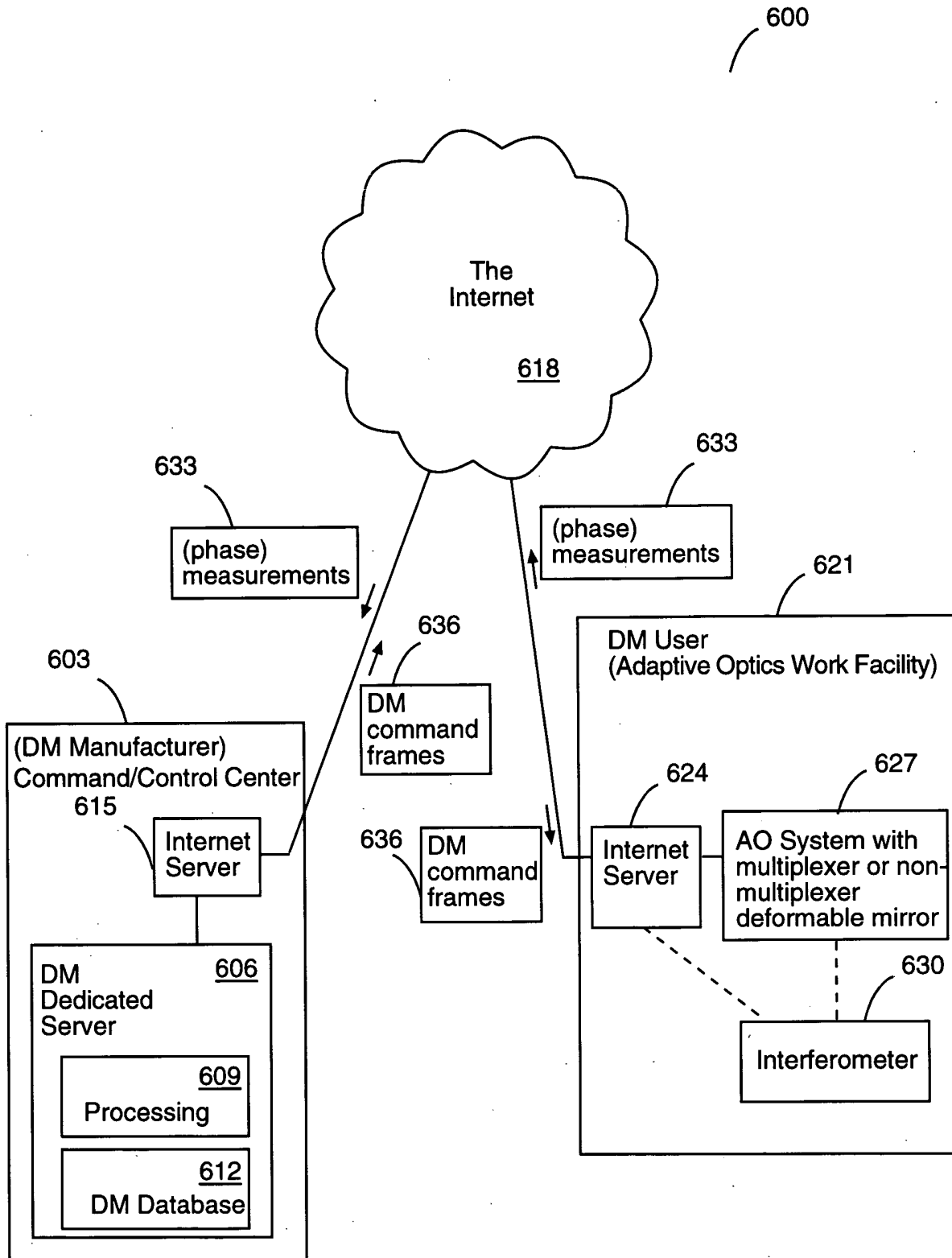


Fig. 31



space-based telescope

639

DM assy

10

642

89a

89b

Command/
Control
Center

603

Fig. 33

